MOSFET – N-Channel, QFET

600 V, 3.0 A, 3.4 Ω

FQP3N60C

Description

This N−Channel enhancement mode power MOSFET is produced using ON Semiconductor’s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 3.0 A, 600 V, $R_{DS(on)} = 3.4\ \Omega$ (Max) @ $V_{GS} = 10$ V, $I_D = 1.5$ A
- Low Gate Charge (Typ. 10.5 nC)
- Low Crss (Typ. 5.0 pF)
- 100% Avalanche Tested
- This is a Pb−Free Device

ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$, unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	600	V
Drain Current	I_D		
Continuous ($T_C = 25°C$)		3	A
Continuous ($T_C = 100°C$)		1.8	A
Drain Current	I_{DM}		
Pulsed (Note 1)		12	A
Gate−Source Voltage	V_{GSS}	±30	V
Single Pulsed Avalanche Energy (Note 2)	E_{AS}	150	mJ
Avalanche Current (Note 1)	I_{AR}	3	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	7.5	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Power Dissipation	P_D		
($T_C = 25°C$)		75	W
Derate above 25°C		0.62	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	−55 to +150	°C
Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds	T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. $L = 30$ mH, $I_{AS} = 3$ A, $V_{DD} = 50$ V, $R_G = 25\ \Omega$, starting $T_J = 25$ °C.
3. $I_{SD} \le 3$ A, di/dt ≤ 200 A/µs, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25$ °C.

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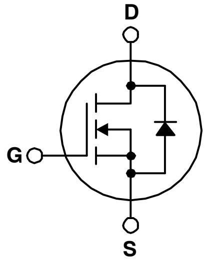
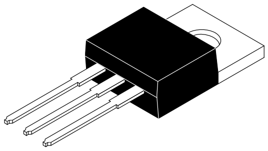
V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
600 V	3.4 Ω @ 10 V	3.0 A

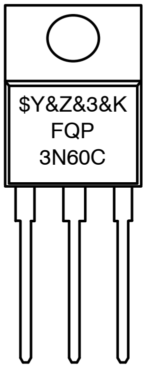


N-CHANNEL MOSFET



TO−220−3LD
CASE 340AT

MARKING DIAGRAM



$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot Code
FQP3N60C = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

August, 2020 − Rev. 3

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP3N60C	FQP3N60C	TO−220−3LD	Tube	N/A	N/A	50 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.67	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	600	–	–	V
ΔBV_{DSS} $/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.6	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 480 V, T_C = 125 °C	–	–	10	
I_{GSSF}	Gate −Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate −Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V			−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 1.5 A	–	2.8	3.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 1.5 A	–	3.5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	435	565	pF
C_{oss}	Output Capacitance		–	45	60	pF
C_{rss}	Reverse Transfer Capacitance		–	5	8	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 3 A, R_G = 25 Ω (Note 4)	–	12	34	ns
t_r	Turn−On Rise Time		–	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		–	35	80	ns
t_f	Turn−Off Fall Time		–	35	80	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 3 A, V_{GS} = 10 V (Note 4)	–	10.5	14	nC
Q_{gs}	Gate−Source Charge		–	2.1	–	nC
Q_{gd}	Gate−Drain Charge		–	4.5	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	3	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	12	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 3 A, dI_F/dt = 100 A/μs	–	260	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.6	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

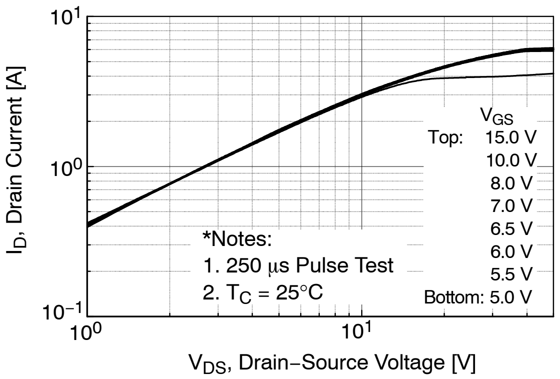


Figure 1. On−Region Characteristics

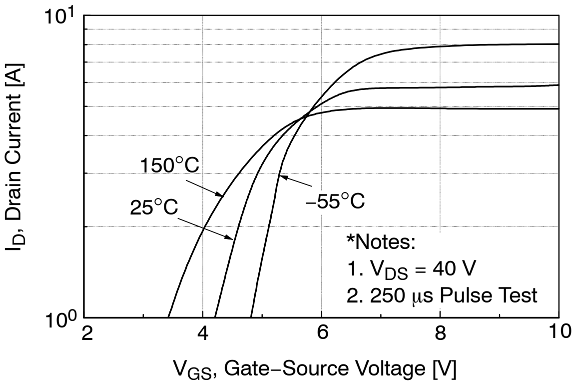


Figure 2. Transfer Characteristics

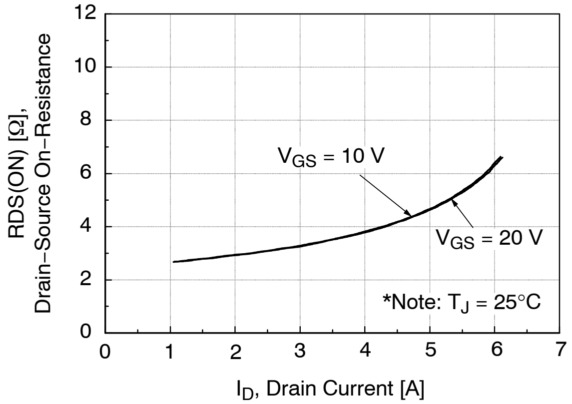


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

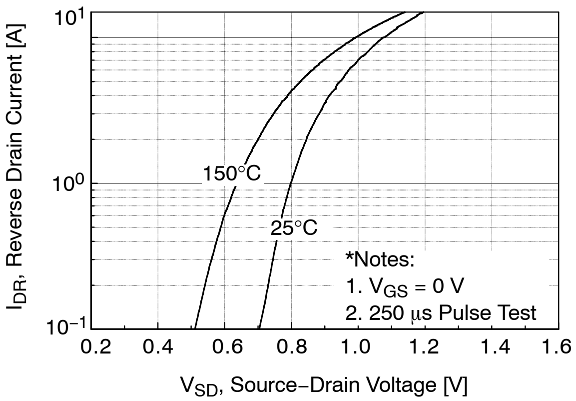


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

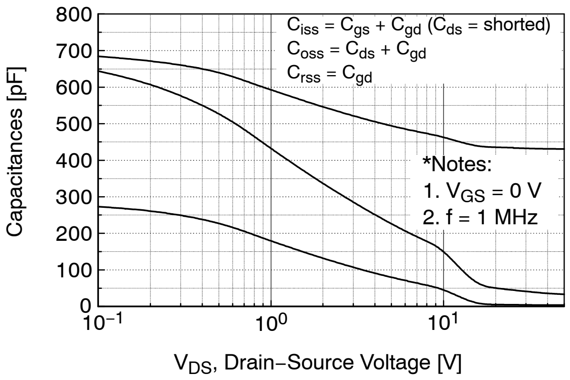


Figure 5. Capacitance Characteristics

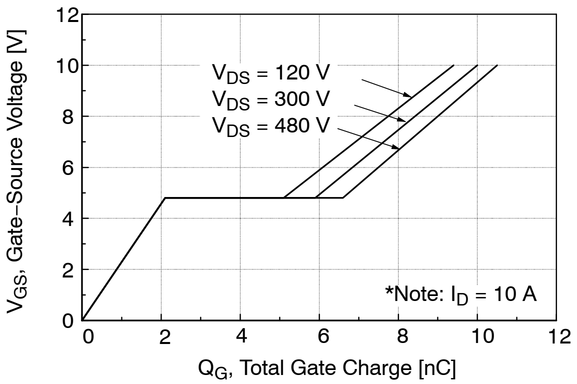
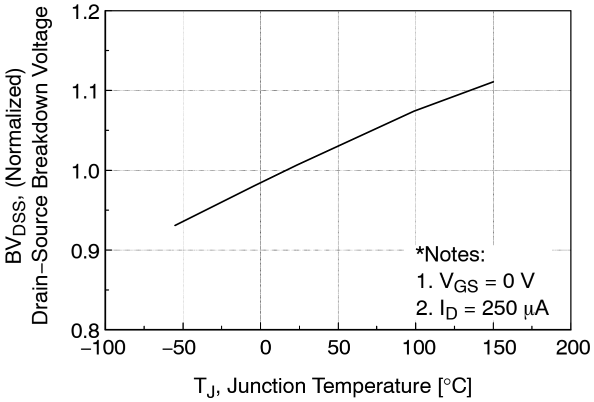


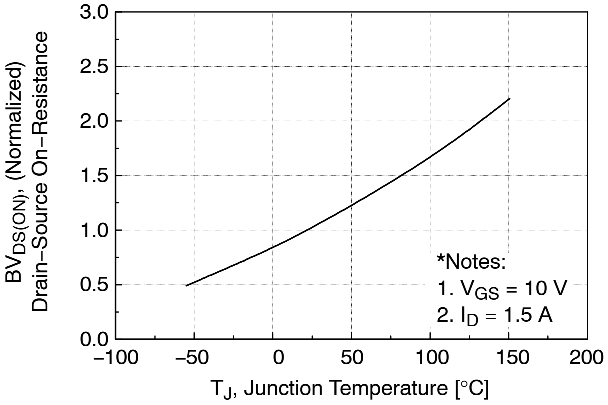
Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS



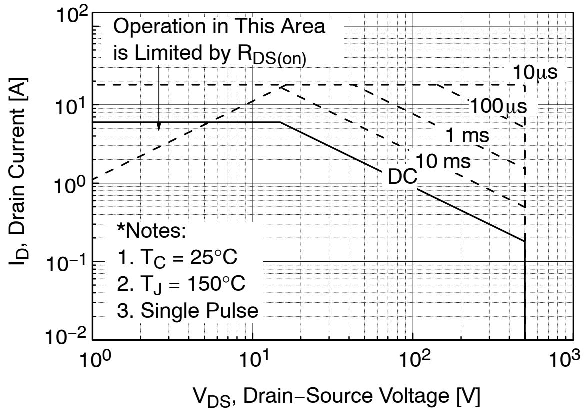
*Notes:
1. V_{GS} = 0 V
2. I_D = 250 μA

Figure 7. Breakdown Voltage Variation vs. Temperature



*Notes:
1. V_{GS} = 10 V
2. I_D = 1.5 A

Figure 8. On−Resistance Variation vs. Temperature



*Notes:
1. T_C = 25°C
2. T_J = 150°C
3. Single Pulse

Figure 9. Maximum Safe Operating Area

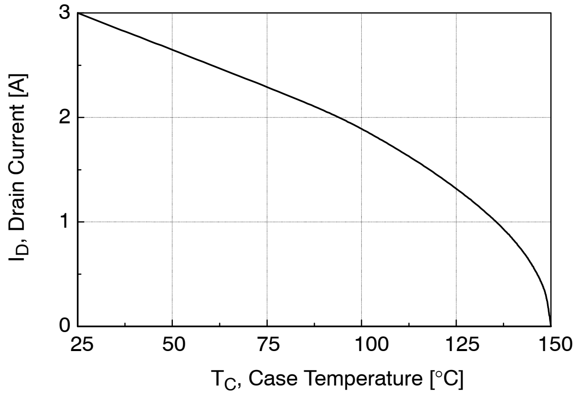
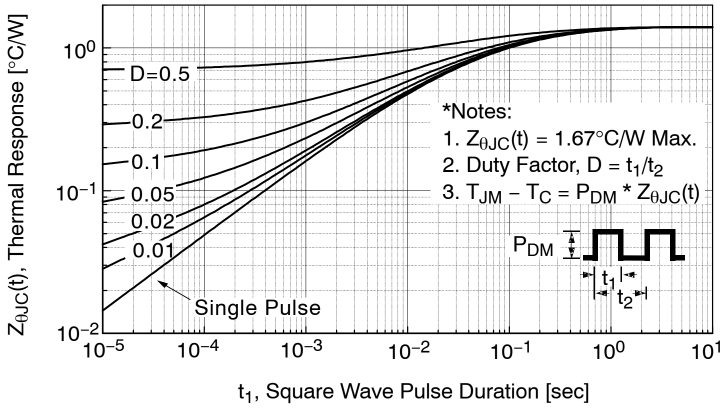


Figure 10. Maximum Drain Current vs. Case Temperature



*Notes:
1. $Z_{\theta JC}(t)$ = 1.67°C/W Max.
2. Duty Factor, $D = t_1/t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

Figure 11. Transient Thermal Response Curve

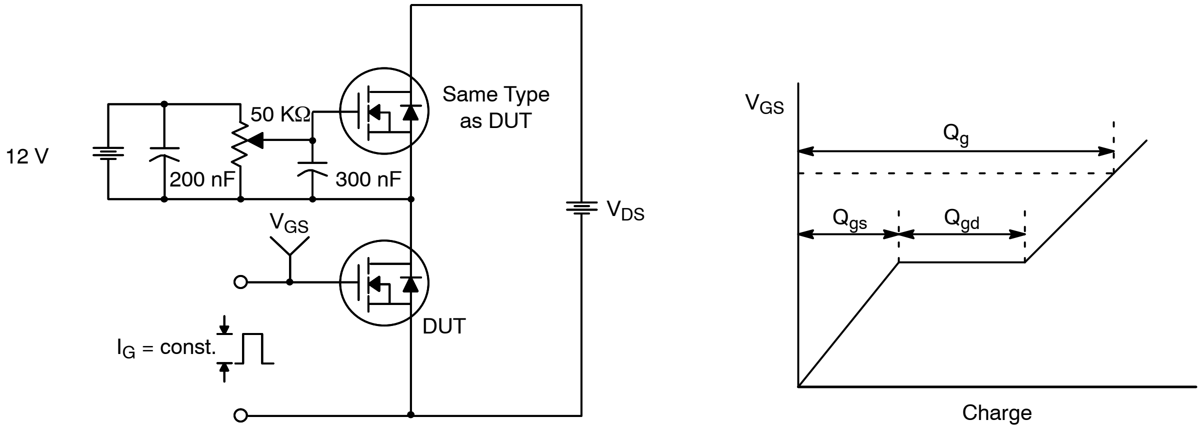


Figure 12. Gate Charge Test Circuit & Waveform

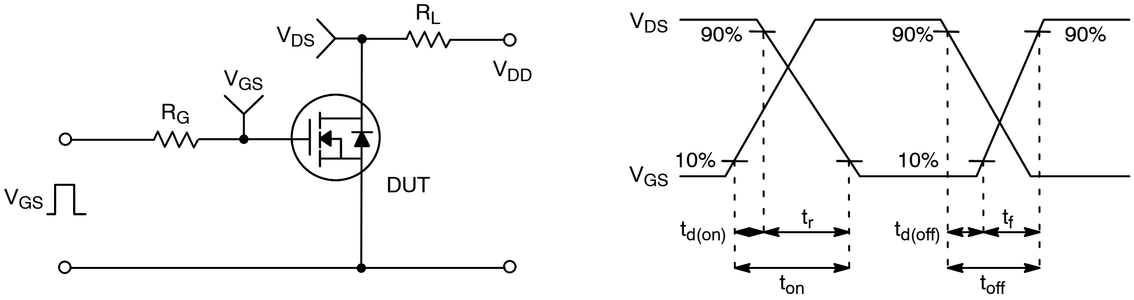


Figure 13. Resistive Switching Test Circuit & Waveforms

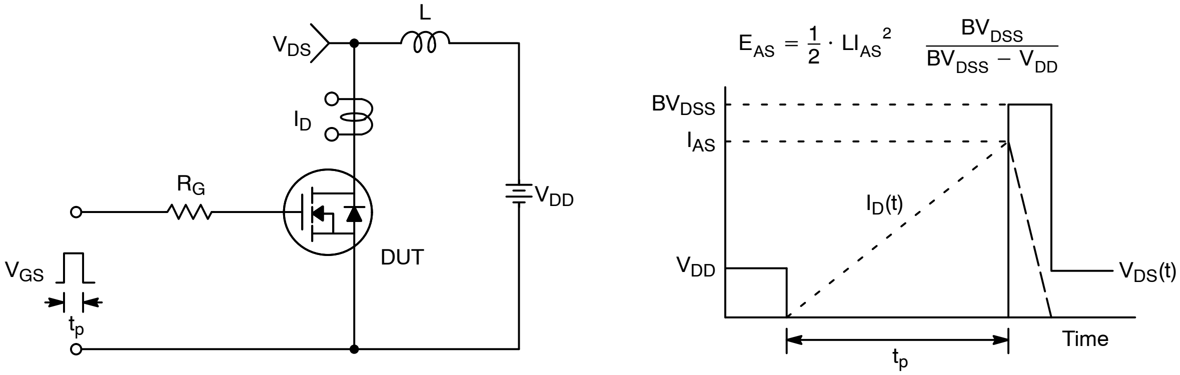


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

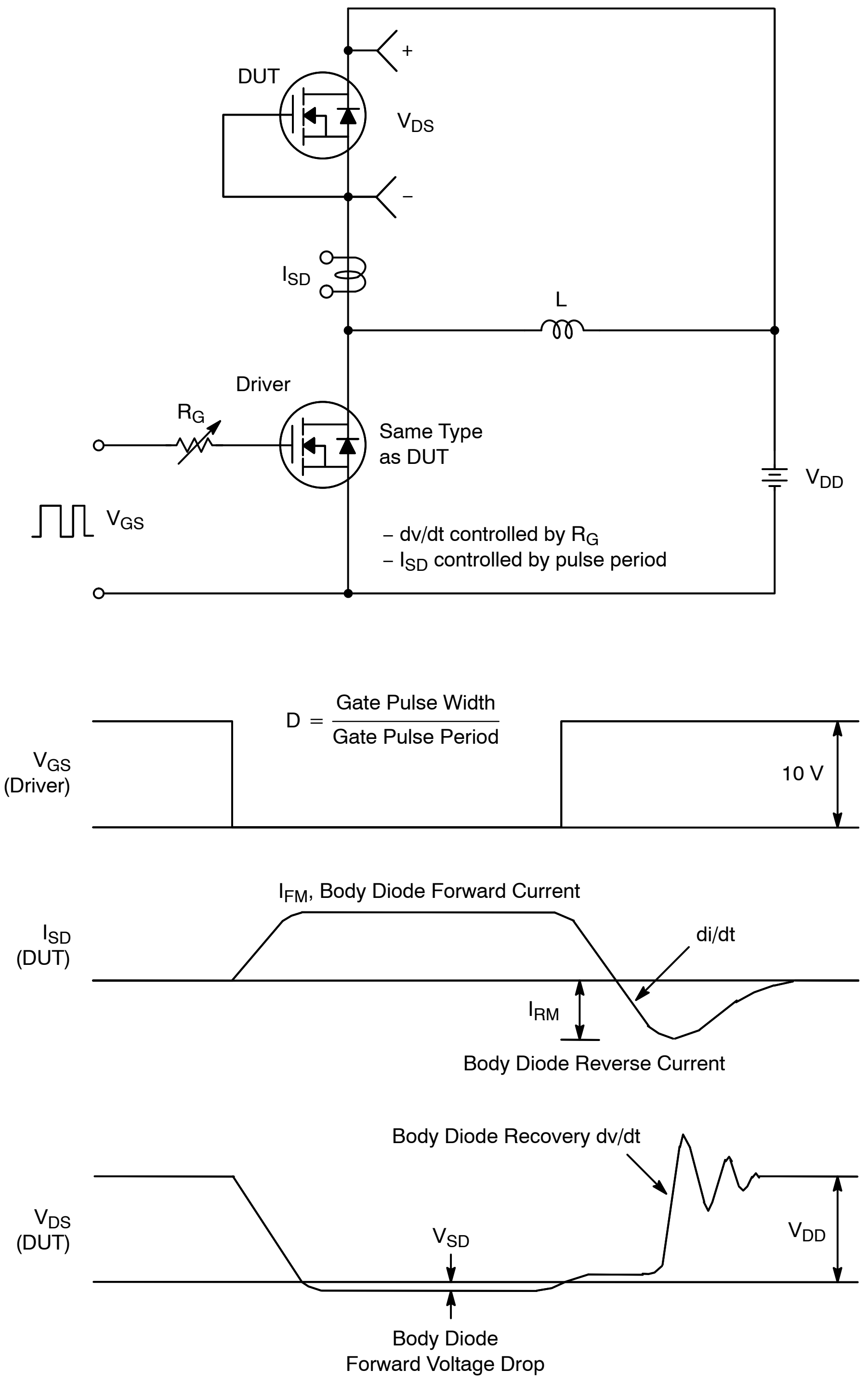


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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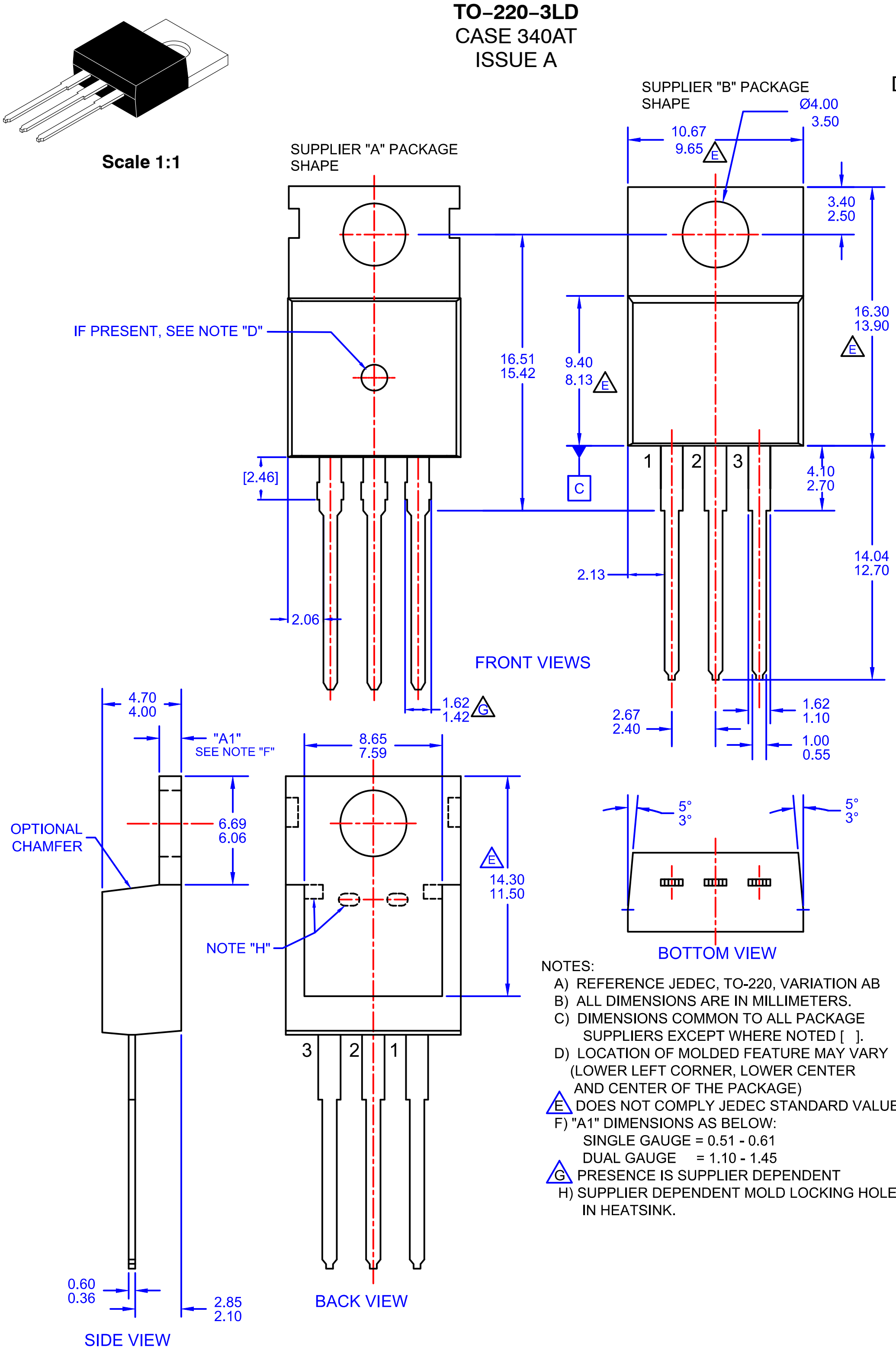
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

Scale 1:1

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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